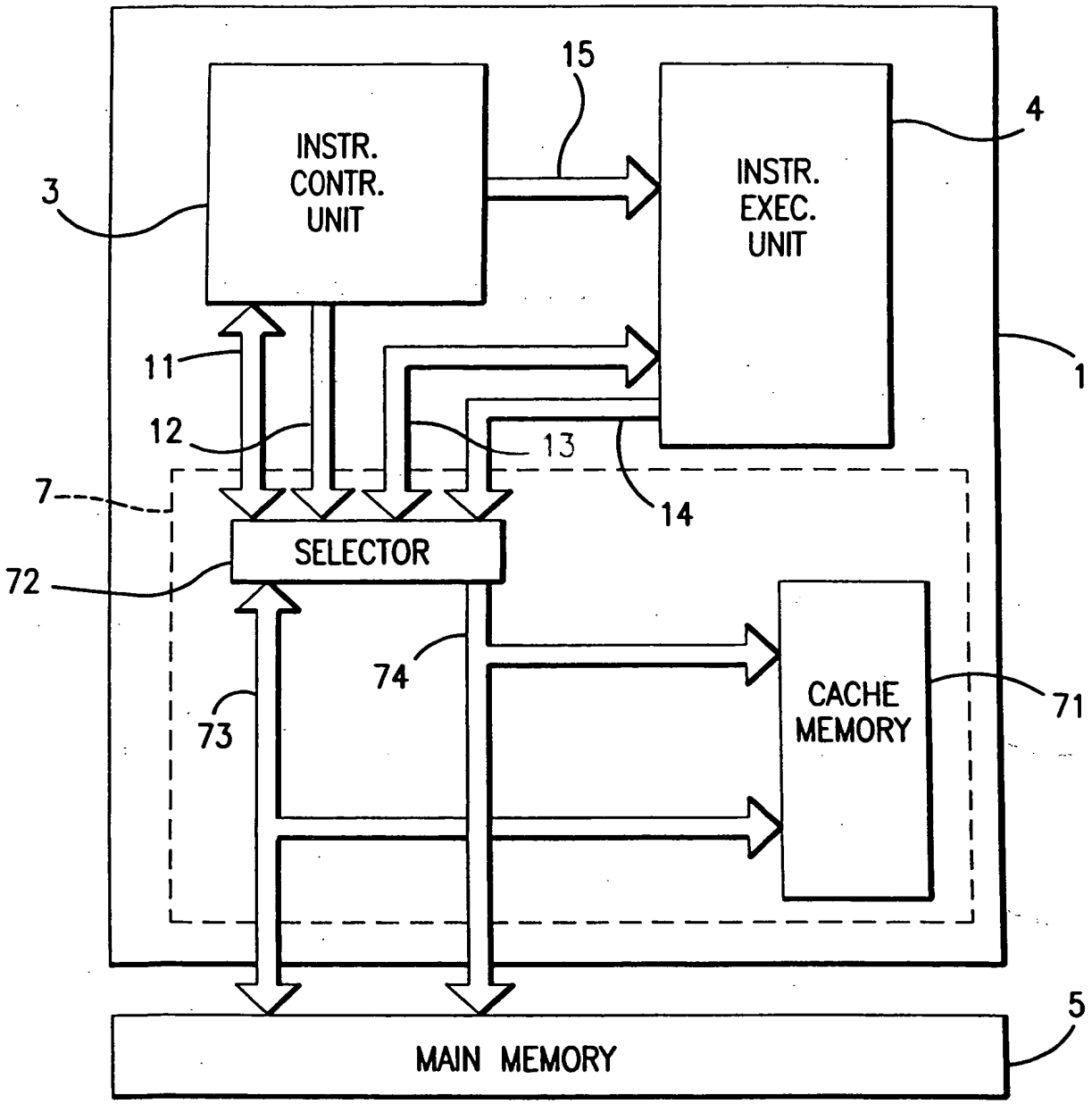

FIG. 1
PRIOR ART

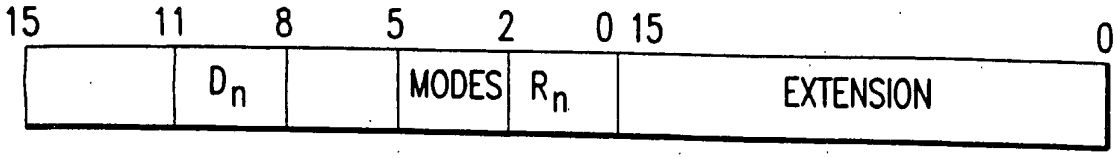

FIG.2A

BITS 5-3	MODES
0 0 0	DATA REGISTER
0 0 1	ADDRESS REGISTER
0 1 0	ADDRESS REGISTER INDIRECT
0 1 1	POST-INCREMENT
1 0 0	PRE-DECREMENT
1 0 1	DISPLACED ADDRESS REGISTER INDIRECT
1 1 0	DISPLACED PROGRAM COUNTER RELATIVE
1 1 1	ABSOLUTE ADDRESS

FIG.2B

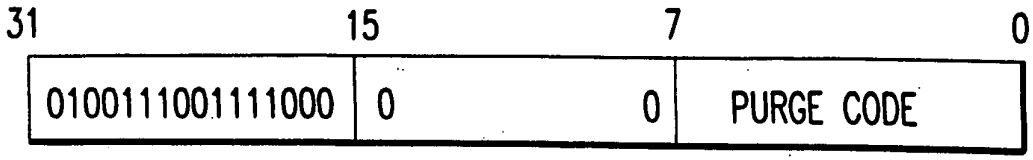

FIG.3A

PURGE CODE	PURGE DESIGNATION
0 0 X X X X X X	RESERVED
0 1 0 0 0 0 0 0	DATA SYSTEM MEMORY
1 0 0 0 0 0 0 0	INSTRUCTION SYSTEM MEMORY
1 1 1 1 1 1 1 1	ALL PURGE

X ··· DON'T CARE

FIG.3B

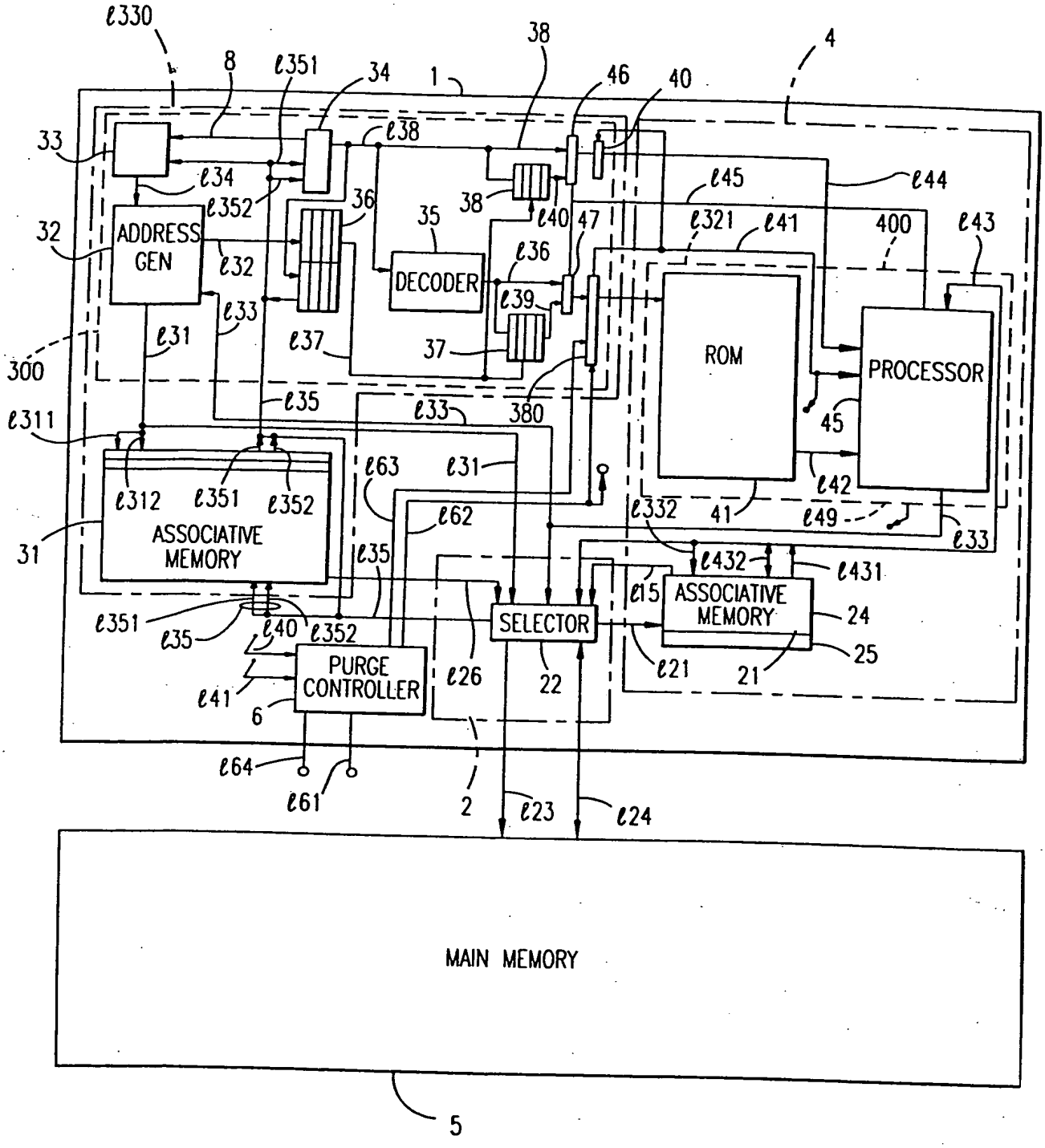
ℓ330
8
ℓ351
34
1
38
46
40
4
33
ℓ38
ℓ34
ℓ352
36
35
38
ℓ40
47
ℓ45
ℓ44
32
ADDRESS GEN
ℓ32
DECODER
ℓ36
ℓ321
ℓ41
400
ℓ43
ℓ33
ℓ39
ROM
PROCESSOR
300
ℓ31
ℓ37
37
380
45
ℓ311
ℓ35
ℓ33
ℓ63
ℓ31
ℓ312
ℓ351
ℓ352
ASSOCIATIVE MEMORY
ℓ42
ℓ332
41
ℓ49
ℓ33
31
ℓ62
ℓ35
ℓ432
ℓ431
ℓ15
ASSOCIATIVE MEMORY
24
ℓ351
ℓ35
ℓ40
ℓ352
SELECTOR
25
PURGE CONTROLLER
ℓ26
22
ℓ21
21
ℓ41
6
ℓ64
ℓ61
2
ℓ23
ℓ24
MAIN MEMORY
5

FIG.4

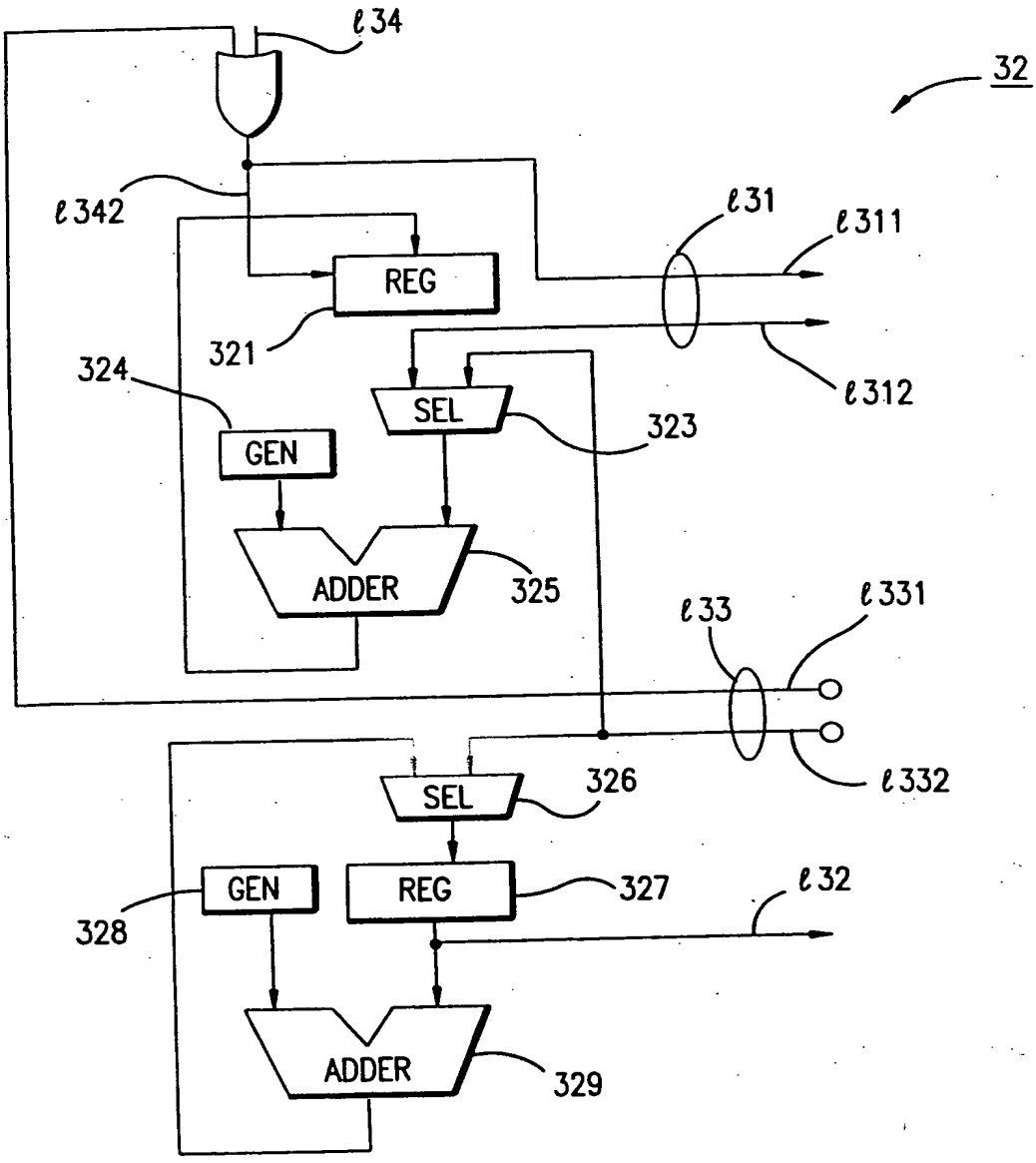
ℓ34
32
ℓ342
ℓ31
ℓ311
REG
321
ℓ312
324
SEL
323
GEN
ADDER
325
ℓ33
ℓ331
ℓ332
SEL
326
GEN
REG
327
ℓ32
328
ADDER
329

FIG.5

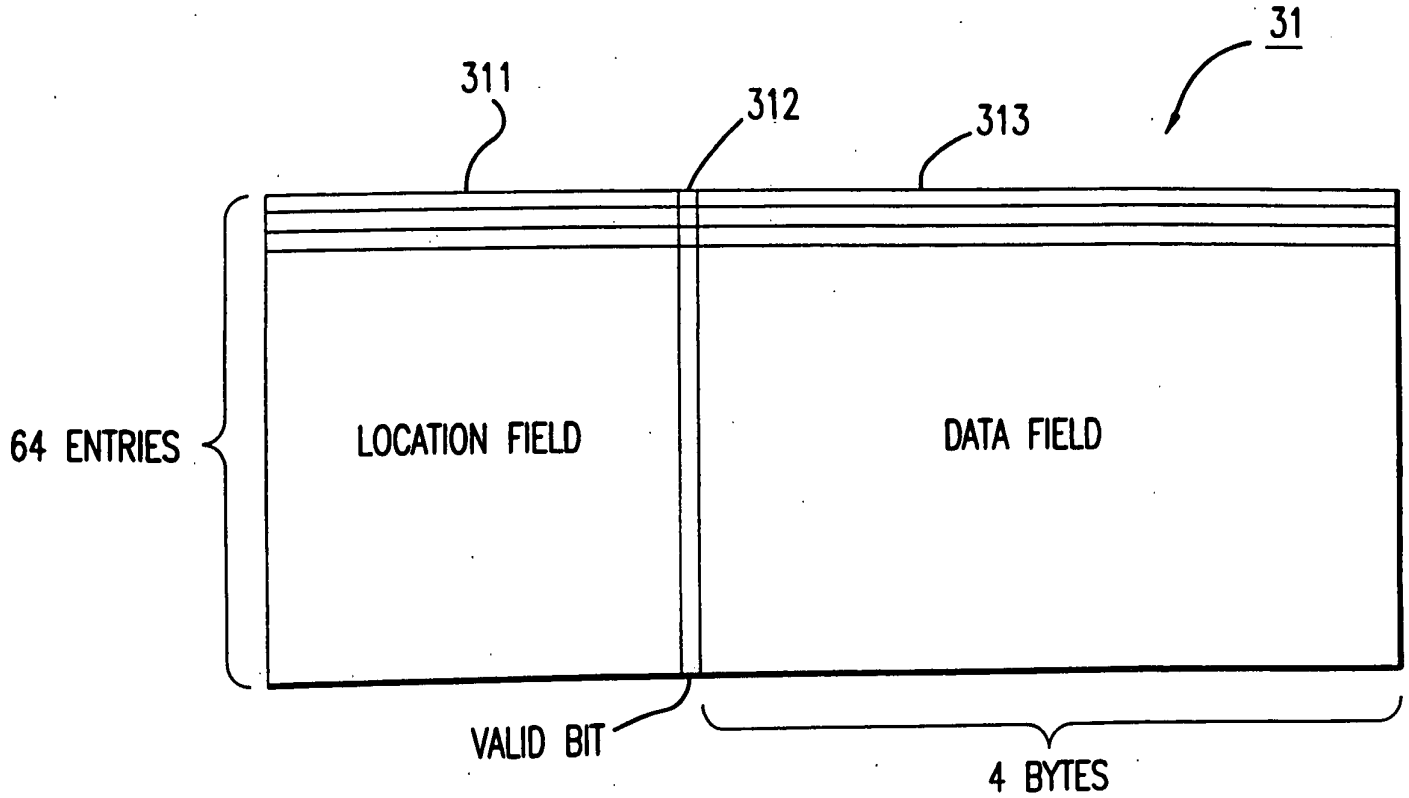
31
311
312
313
64 ENTRIES
LOCATION FIELD
DATA FIELD
VALID BIT
4 BYTES

FIG.6

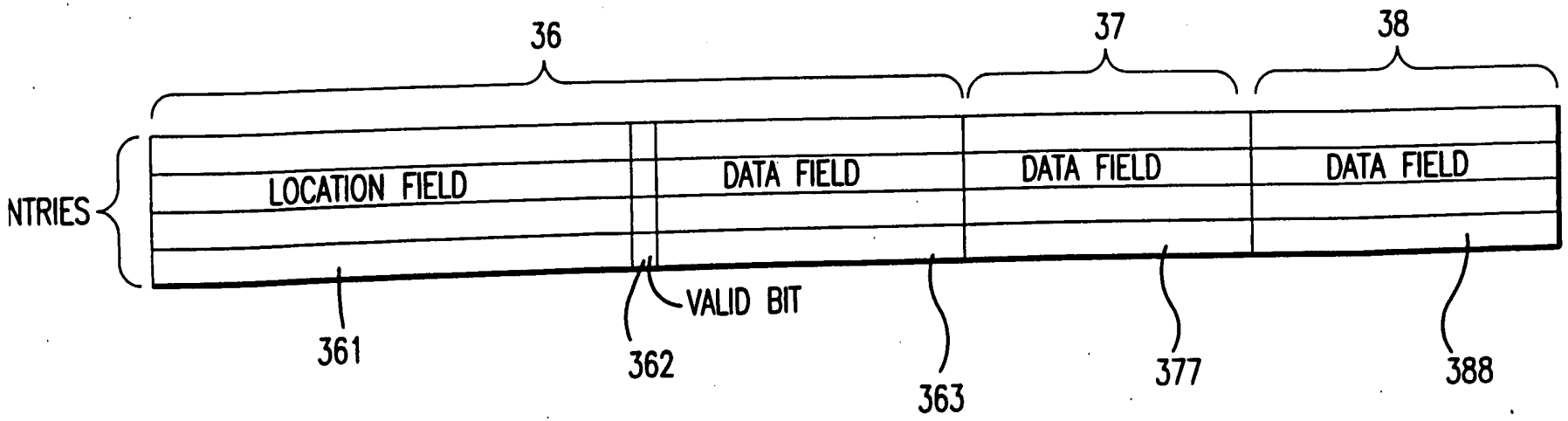
36
37
38
NTRIES
LOCATION FIELD
DATA FIELD
DATA FIELD
DATA FIELD
VALID BIT
361
362
363
377
388

FIG.7

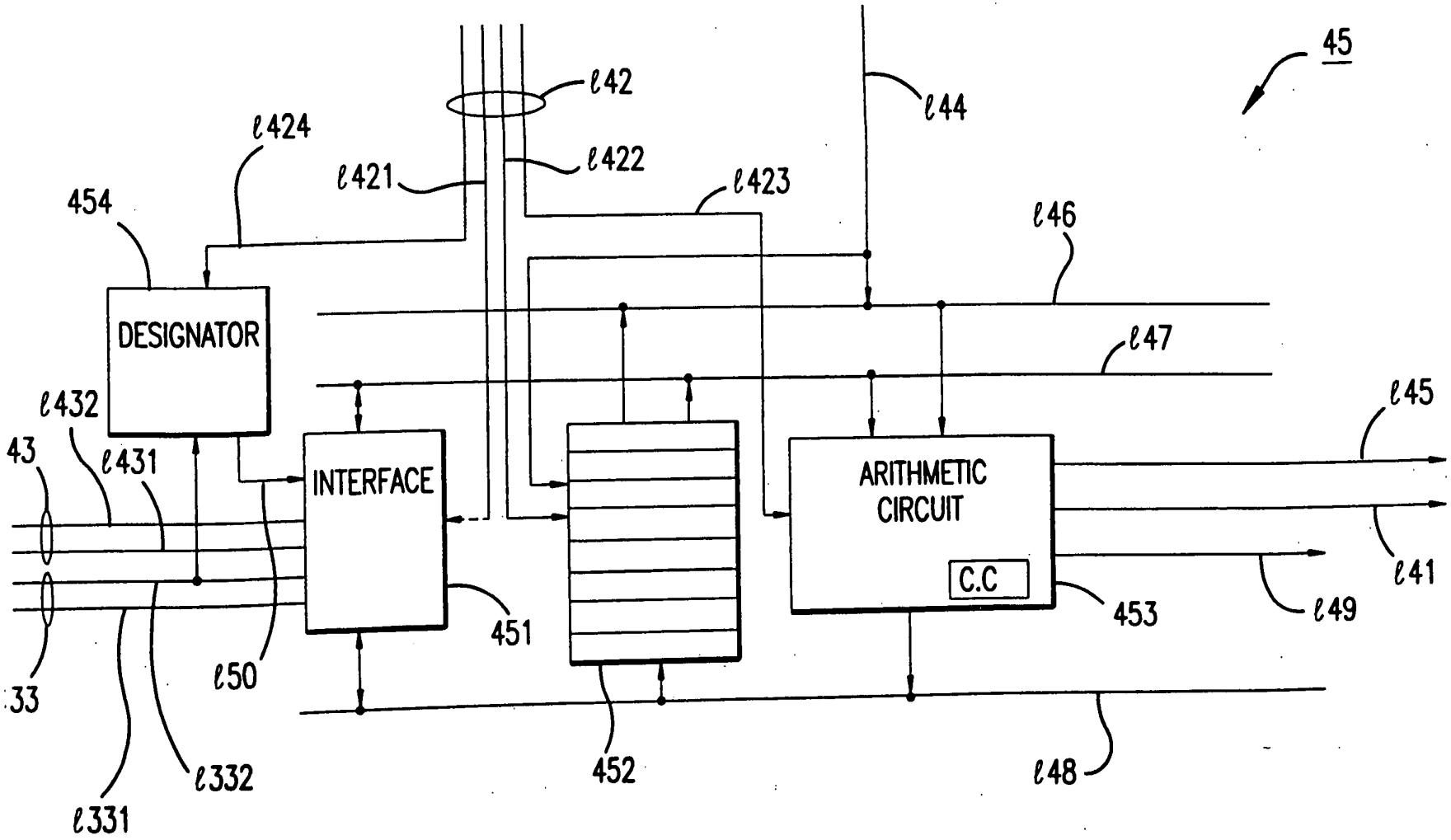
45
ℓ42
ℓ44
ℓ424
ℓ421
ℓ422
ℓ423
454
ℓ46
DESIGNATOR
ℓ47
ℓ432
ℓ45
43
ℓ431
INTERFACE
ARITHMETIC
CIRCUIT
C.C
ℓ41
ℓ49
453
451
ℓ50
33
ℓ332
ℓ331
452
ℓ48

FIG.8

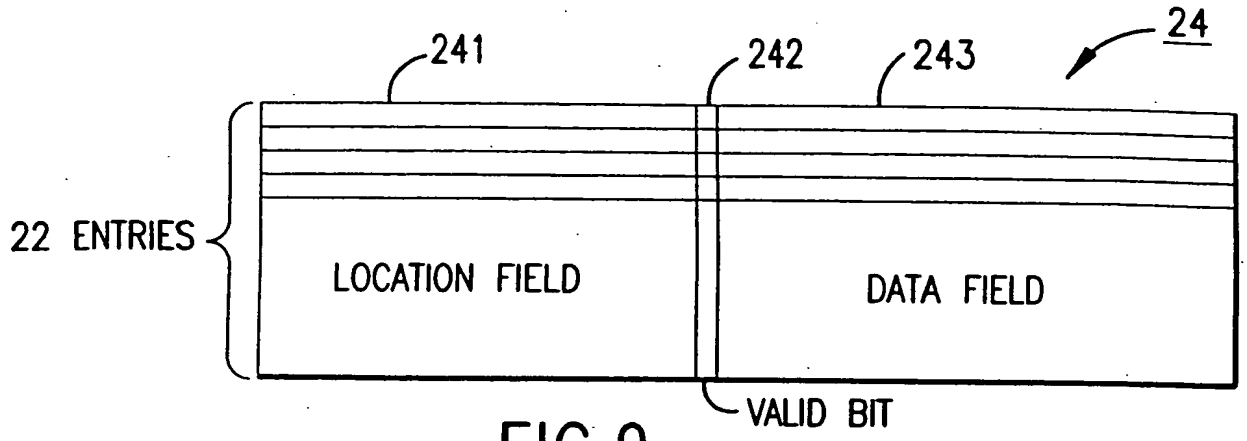

FIG.9

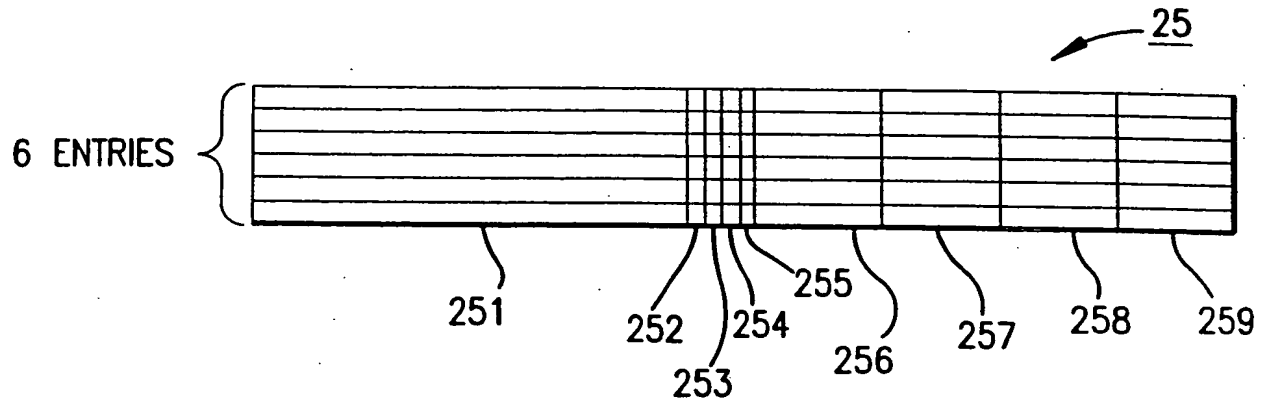

FIG.10

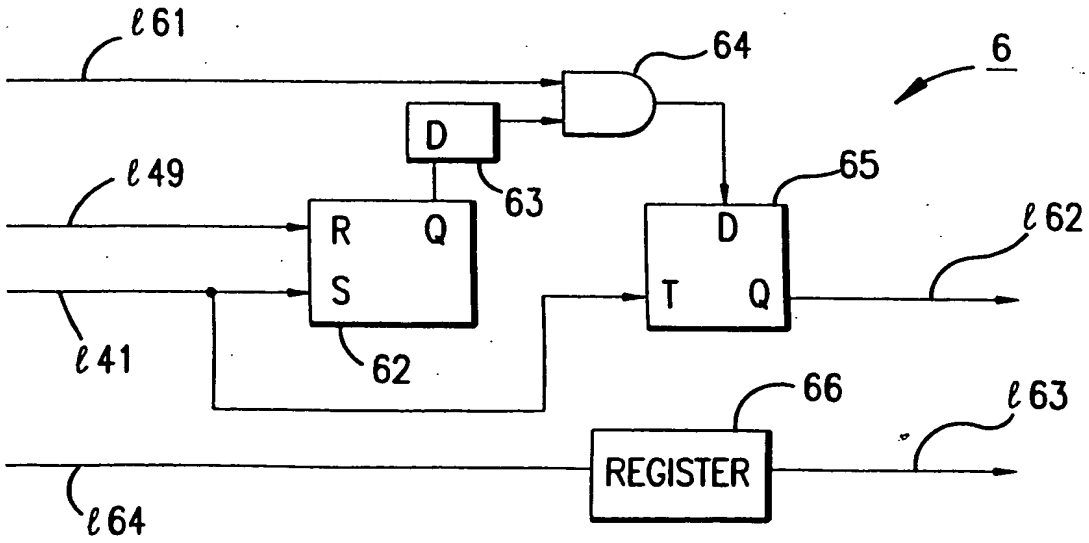

FIG 12

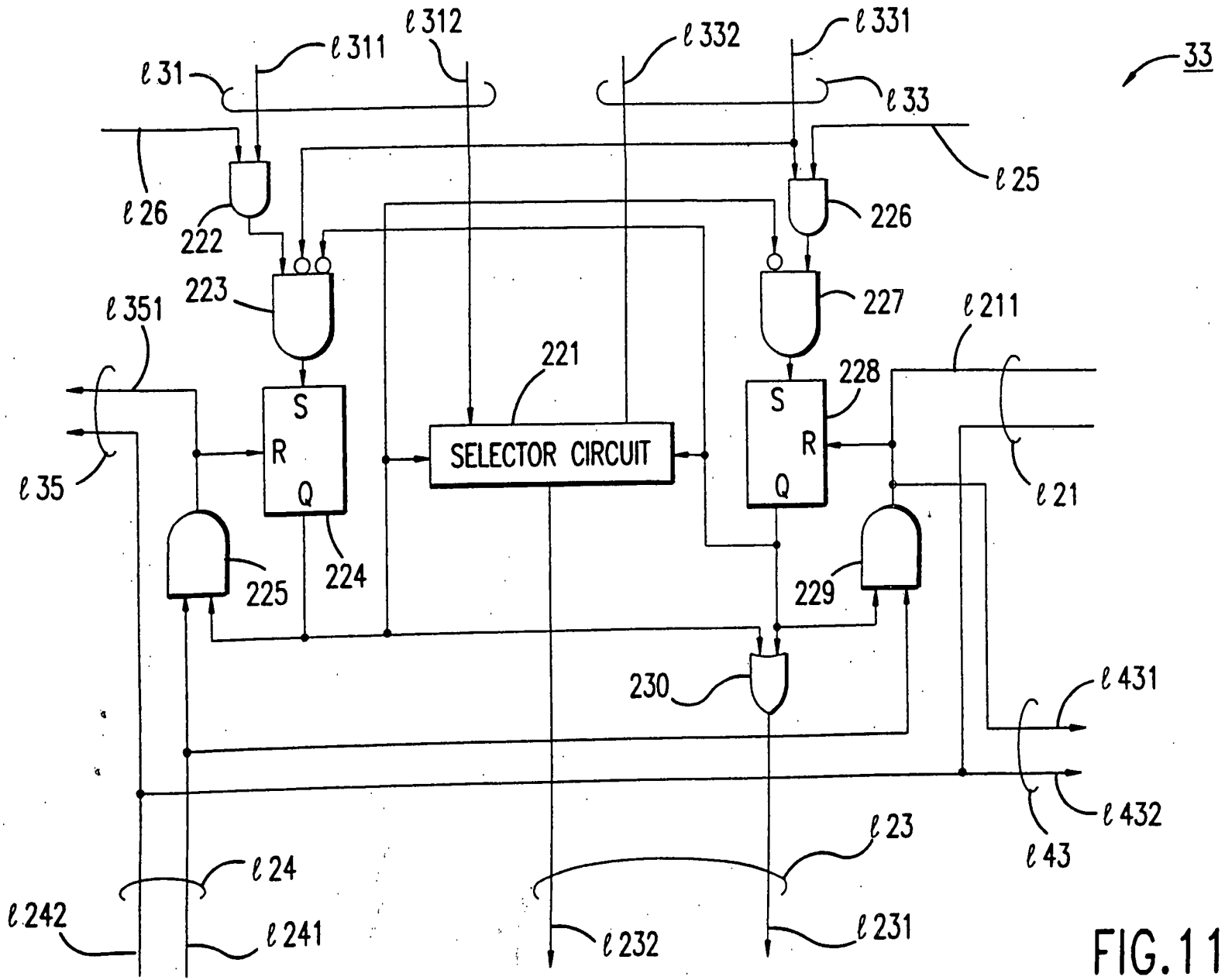
ℓ 312
ℓ 311
ℓ 31
ℓ 332
ℓ 331
33
ℓ 33
ℓ 25
ℓ 26
222
226
223
227
ℓ 351
ℓ 211
221
228
S
R
Q
SELECTOR CIRCUIT
S
R
Q
ℓ 35
ℓ 21
225
224
229
230
ℓ 431
ℓ 432
ℓ 43
ℓ 23
ℓ 24
ℓ 242
ℓ 241
ℓ 232
ℓ 231

FIG.11

NO.	ADDRESS MODES	PROCESS
NO.1	ADDRESS REGISTER INDIRECT	FETCH
NO.2	ADDRESS REGISTER INDIRECT	FETCH
NO.3	DATA REGISTER	ADD
NO.4	ADDRESS REGISTER	STORE
NO.5	ADDRESS REGISTER	JUMP TO NO.10
NO.6		
NO.7		
NO.8		
NO.9		
NO.10	DATA REGISTER	ADD
NO.11		

FIG.13

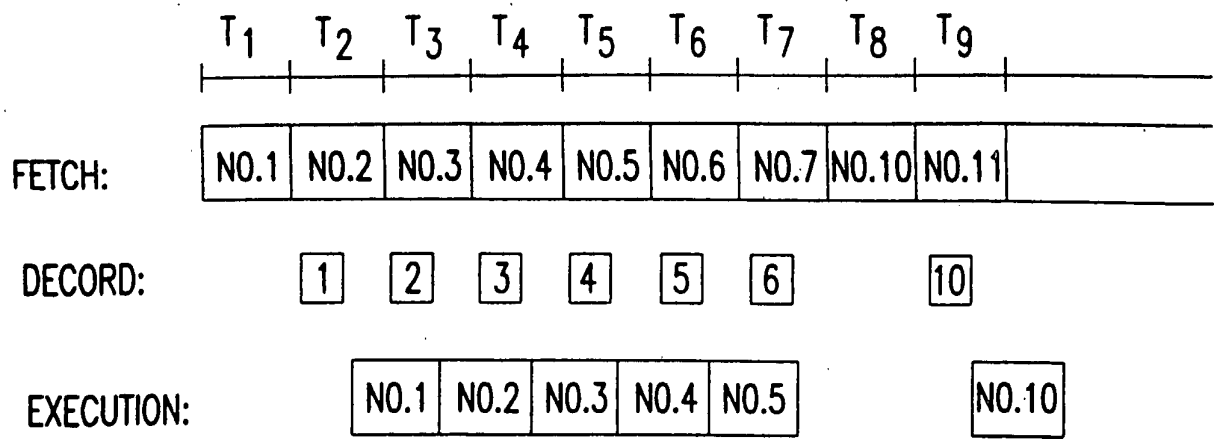

FIG.14A

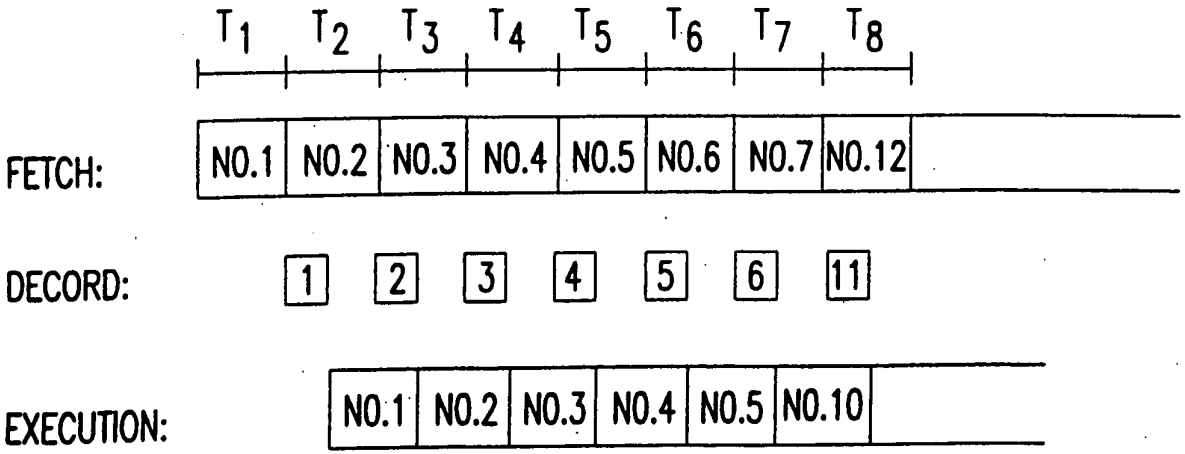

FIG.14B